IN THE CLAIMS

Cancel claims 1-20 without prejudice or disclaimer, and add new claims 21-46 as follows.

1-20. (Canceled).

21. (New) A computer system comprising:

a processor generating an address of a virtual address system,

a first main memory storing information which said processor processes,

a non-volatile storage storing first memory size information of said first main memory and second memory size information of a second main memory that is to be hot-added, and a case housing said processor, said first main memory, and said non-volatile storage.

22. (New) A computer system according to claim 21,

wherein said processor has an address translating unit translating virtual addresses and physical addresses and

said processor outputs physical addresses representing a region of said first main memory.

23. (New) A computer system according to claim 21,

wherein said main memory stores at least a part of a first page structure of said region for said first main memory and

has a region for a second page structure of said second and

has a region for a second page structure of said second main memory, and

wherein said processor accesses said first main memory using said first page structure.

24. (New) A computer system according to claim 21,

wherein said non-volatile storage is EEPROM.

25. (New) A computer system according to claim 21, further comprising:

a connecting switch connecting said processor, said first main memory and said non-volatile storage.

26. (New) A computer system supporting a virtual memory system, said computer system comprising,

a processor,

a first main memory which said processor accesses,

a non-volatile storage storing configuration information regarding a second main memory to be hot plugged, and

a housing including said processor, said first main memory and said non-volatile storage.

27. (New) A computer system according to claim 22,

wherein said configuration information has memory size information of a memory enabled to be hot plugged as said second main memory.

28. (New) A computer system according to claim 22,

wherein said first main memory has at least a part of address translation information of said first main memory.

29. (New) A computer system according to claim 22,

wherein said first main memory has at least a part of address translation information of said first main memory and has a first region in which address translation information for said second main memory is to be stored,

wherein said processor has a unit translating logical-physical addresses, accesses said address translation information for said first main memory and generates physical addresses.

30. (New) A computer system according to claim 29, wherein said first main memory stores said address translation information for said first main memory in a top priority region of interrupt handling and assigns said first region in said top priority region.

31. (New) A computer system according to claim 29, further comprising a connecting switch connecting said processor and said first main memory.

32. (New) A computer system comprising,

a first main memory,

a processor processing information stored in said first main memory,

a non-volatile storage storing memory information of a second memory to be hot-inserted while said computer system being powered, and

a housing including said first main memory, said processor, and said non-volatile storage.

33. (New) A computer system according to claim 32, wherein said non-volatile storage stores memory size information of said second main memory as said memory information.

34. (New) A computer system according to claim 32, wherein said non-volatile storage stores memory size information of said first main memory.

35. (New) A computer system according to claim 32, wherein said first main memory has at least part of first logical-physical address translating pairs of said first main memory and has an assigned region to store second logical-physical address translating pairs of said second main memory, and

wherein said first logical-physical address translating pairs are used for said processor accessing said first main memory.

36. (New) A computer system according to claim 35, wherein said processor has a logical-physical address translating unit and said logical-physical address translating unit uses said first logical-physical address

translating pairs when said processor accesses said first main memory.

37. (New) A computer system according to claim 35, wherein said first main memory has an untranslatable region and stores said first logical-physical address translating pairs in said untranslatable region.

38. (New) A computer system according to claim 37, wherein said first main memory has an untranslatable region and stores said first logical-physical address translating pairs in said untranslatable region.

39. (New) A computer system according to claim 32, wherein said non-volatile storage is EEPROM.

40. (New) A computer system according to claim 32, further comprising a connecting switch connecting said processor and said first main memory.

41. (New) A computer system, allowing a main memory to be hot-added while said computer system is powered on, comprising,

a first main memory,

a processor accessing said first main memory with a virtual memory system,

a non-volatile storage storing size information of main memory to be hot-added while powered on, and

a body housing said first main memory, said processor and said non-volatile storage.

42. (New) A computer system according to claim 41, wherein said non-volatile storage is EEPROM.

43. (New) A computer system according to claim 41, further comprising a connecting switch connecting said processor and said first main memory.

44. (New) A computer system according to claim 41, wherein said first main memory has a first logical-physical address translating table for said first main memory, and

further has a region to store a second logical-physical address translating table for said main memory to be hot added.

45. (New) A computer system according to claim 41, wherein said first main memory has an untranslatable region and stores said first logical-physical address translating table in said untranslatable region.

46. (New) A computer system according to claim 41, wherein said first main memory further assigns said region to store a second logical-physical address translating table for said main memory to be hot-added in said untranslatable region.